REMARKS

Claims 1-15 are pending in this application. Claims 1-3, 5-6, 10 and 13-15 have been amended to address the Examiner's objections. Figure 5 has been amended to correct a typographical error. Favorable reconsideration is respectfully requested.

Claims 1-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kochi et al.* (U.S. Patent 6,166,583) in view of *Ogawa et al.* (U.S. Patent 5,926,057). Applicant respectfully traverses this rejection, because the cited references, alone or in combination, do not disclose or suggest features of the outputting units or outputting step of the present invention as described in independent claims 1 and 6.

More specifically, claim 1 describes a plurality of outputting units, each for receiving a result of the operation of a corresponding one of operating units and outputting the result of the operation for each of the corresponding one of a plurality of elements that are disposed in a matrix of an optical area (see Fig. 4). Claim 6 also describes this feature in a method format.

The *Kochi et al.* reference discloses an arithmetic operation output 50 (see FIG. 19A and 19B) provided in a chip arrangement for performing high-speed image processing. The chip arrangement also includes an image data sensing unit 60 having rows and columns of light-receiving portions or pixels 41. As noted by the Examiner (Office Action page 4, line 10), the chip arrangement of *Kochi et al.* uses a single output, rather than a plurality of outputting units for all the numerous pixels of the sensing unit. Thus, the *Kochi et al.* reference does not disclose or suggest the plurality of outputting units corresponding to the plurality of operating units of the present invention.

However, the Examiner asserted that "Ogawa implies a plurality of . . . outputting units" (see Office Action, page 4, second paragraph, lines 7-8), and went further to conclude that it would have been obvious to incorporate the teaching implicated by *Ogawa et al.* Applicant respectfully submits that reliance upon *Ogawa et al.* in this regard is improper. *Ogawa* does not teach "a plurality of outputting units, each for receiving a result of the operation of a corresponding one of said operating units and outputting the result of the operation for each of said corresponding one of said elements" as recited in claim 1 (and recited in method format in claim 6), but generally recognizes that parallel processing may be obtained using a plurality of

semiconductor chips (col. 1, lines 33-40). This clearly does not teach the limitations recited in the aforementioned claims, since such a configuration is not being claimed.

Furthermore, the above passage in the *Ogawa et al.* reference relied upon by the Examiner teaches away from the disclosure in *Kochi et al.* By combining semiconductor chips in the way suggested by the Examiner, the proposed modification would render the *Ogawa* and *Kochi* references unsatisfactory for their intended purposes, since the teachings in both references disparage the use of multiple semiconductor chips (see *Kochi et al.*, col. 1, lines 21-30; *Ogawa et al.* col. 1, lines 41-45). Accordingly, there can be no suggestion or motivation to make the proposed modification (see MPEP 2143.01), and such comparison ignores the requirement that the invention must be considered as a whole when ascertaining differences between the prior art and the claimed invention (see MPEP 2141.02).

Kochi also does not teach the timing adjustment means/step limitations of claims 1 and 6. The passage relied upon by the Examiner (col. 11, lines 9-12) teaches a timing and polarity signal (S3) that is used to adjust the signal application timings between a weighted input and other input terminals of the arithmetic operation circuit block (col. 11, lines 35-38). Accordingly, it does not teach a timing adjustment where "the result of the operation is output for each of said plurality of elements from said outputting units" as cited in claim 1 and similarly recited in claim 6.

Furthermore, *Kochi* does not teach or suggest the timing means using a "control signal other than the clear signal or the transfer signal in the timing adjustment" as cited in claim 1 and similarly recited in claim 6. The clear signal and transfer signal that is disclosed in *Kochi* (col. 8, lines 57-60) are both used to control latching in the arithmetic operating circuit (701-A et al). The control signal cited by the Examiner (col. 4, lines 59-67) is expressly used to control latching in the semiconductor device of FIG. 2 (col. 4, lines 41-67), and has no relation to the transfer signals used in the arithmetic operating circuit. Such nonanalogous combination of references is proscribed by MPEP 2141.01(a). For at least these reasons, claims 1 and 6, and their dependent claims 2-5, 7-10 and 13-15 are allowable over the cited references.

In addition to the above arguments, Applicant respectfully traverses with respect to claims 11 and 12 because the cited references, alone or in combination, do not disclose or suggest the features of the present invention in which the operation of the operating means

includes a plurality of modes which are represented by different expressions from each other, as described in claims 11 and 12. The Examiner asserts that *Ogawa* implies a plurality of modes represented by different expressions from each other (col. 3, lines 32-38). However, this is incorrect and misstates the teaching of *Ogawa*. The passage relied upon by the Examiner discloses that the number of parallel processing stages may be increased by slave-connecting semiconductor devices to realize various arithmetic operations (col. 3, lines 26-38). This clearly is outside of the scope of the aforementioned limitations, since there is no such configuration is recited in the claims. For at least these reasons, claims 11 and 12 are also allowable over the cited references.

In light of the above, Applicant respectfully submits that claims 1-15 are now in condition for allowance, which is respectfully requested.

Respectfully submitted,

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